TS128MDR72V6L5

184Pin DDR266 1U Registered DIMM
1GB With 64Mx4 CL2.5

Description

The TS128MDR72V6L5 is a Low Profile 128M x 72bits Double Data Rate SDRAM high-density for PC-266. The TS128MDR72V6L5 consists of 36pcs CMOS 64Mx4 bits Double Data Rate SDRAMs in 66 pin TSOP-II 400mil packages, 2pcs drive ICs for input control signal, 1pcs PLL, and a 2048 bits serial EEPROM on a 184-pin printed circuit board. The TS128MDR72V6L5 is a Dual In-Line Memory Module and is intended for mounting into 184-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

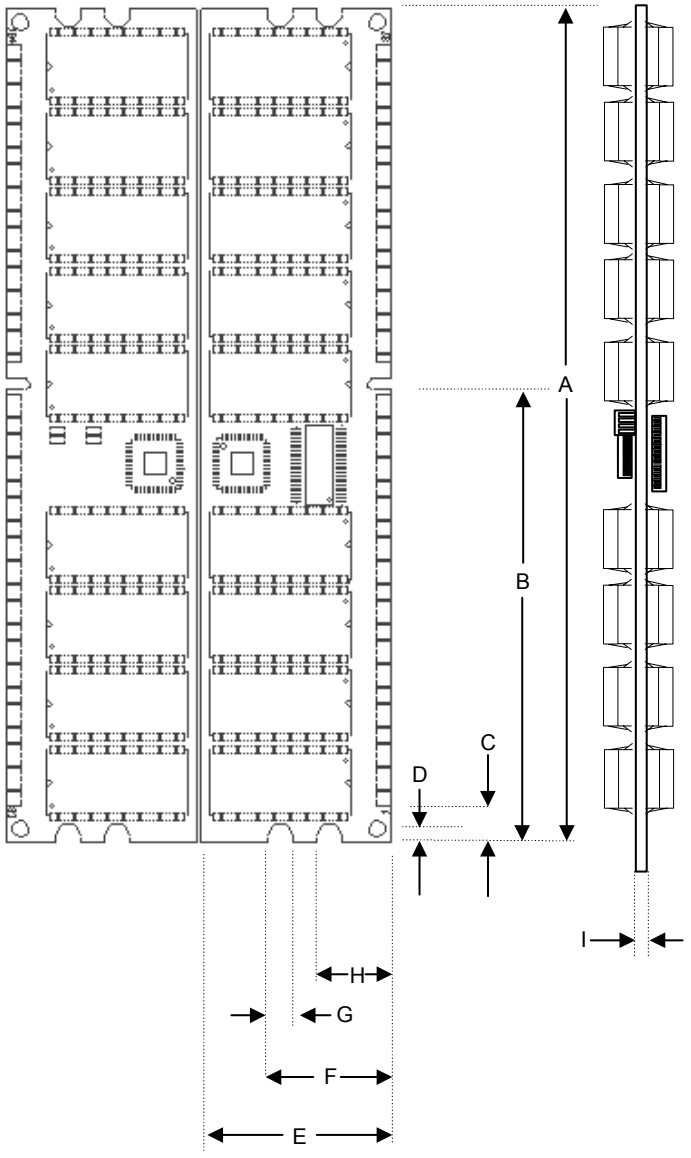
- Power supply: VDD: 2.5V ± 0.2V, VDDQ: 2.5V ± 0.2V
- Max clock Freq: 133MHZ.
- Burst Mode Operation.
- Auto and Self Refresh.
- All inputs except data & DM are sampled at the positive going edge of the system clock (ck).
- Data I/O transactions on both edge of data strobe.
- Edge aligned data output, center aligned data input.
- Serial Presence Detect (SPD) with serial EEPROM
- SSTL-2 compatible inputs and outputs.
- MRS cycle with address key programs.

  CAS Latency (Access from column address): 2.5

  Burst Length (2,4,8)

  Data Sequence (Sequential & Interleave)

Placement



PCB: 09-1380

Dimensions

Side	Millimeters	Inches
A	133.35±0.20	5.250±0.008
B	72.39	2.850
C	6.35	0.250000
D	2.20	0.0870
E	30.48±0.20	1.20±0.00800
F	19.80	0.779
G	4.00	0.157
H	12.00	0.472
I	1.27±0.10	0.050±0.004

Pin Identification

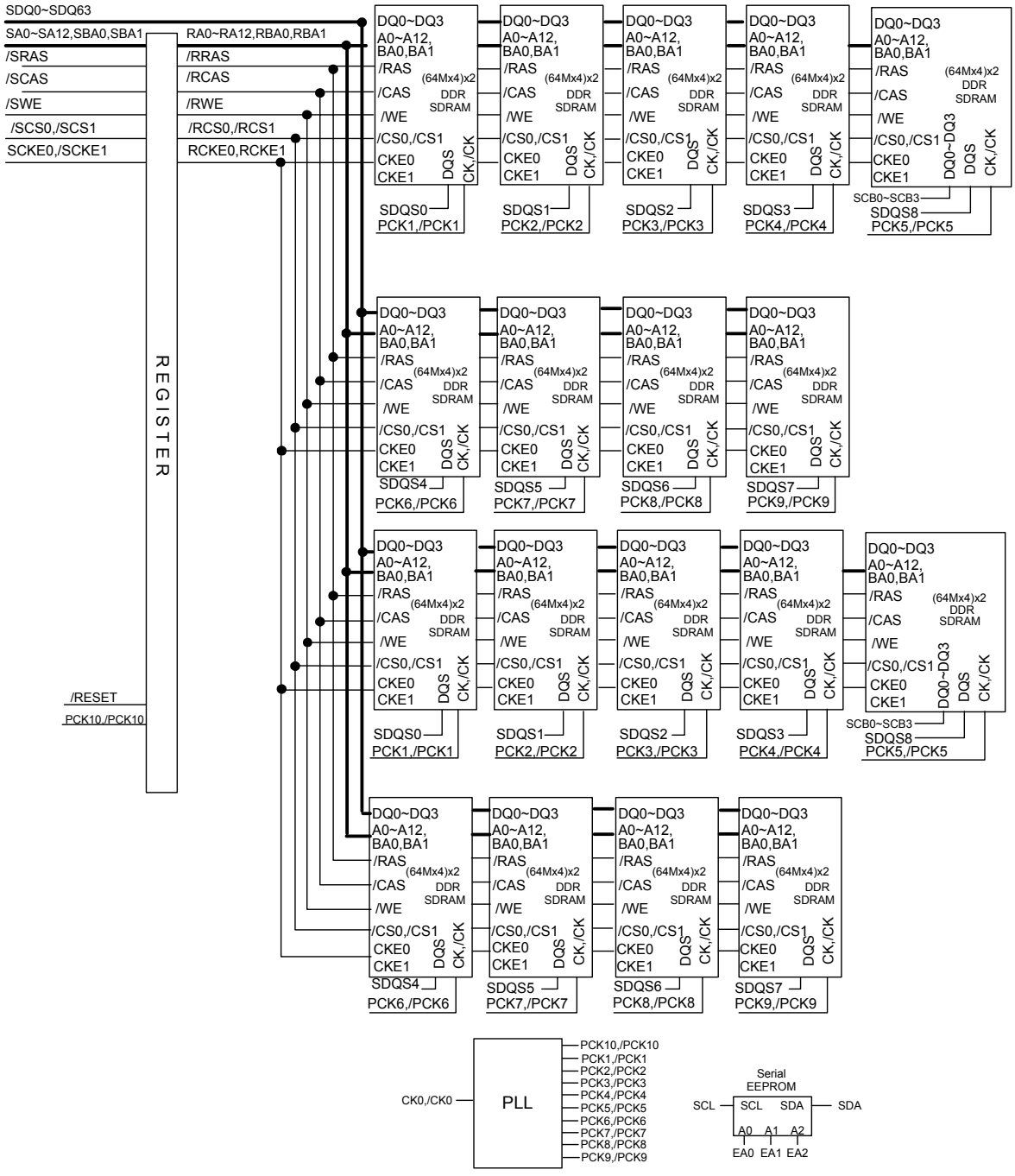
Symbol	Function
SA0~SA12, SBA0, SBA1	Address input
SDQ0~SDQ63	Data Input / Output.
SCB0~SCB7	Check bit
SDQS0~SDQS8, SDM0~SDM8	Data strobe input/output
CK0, /CK0	Clock Input.
SCKE0, SCKE1	Clock Enable Input.
/SCS0, /SCS1	Chip Select Input.
/SRAS	Row Address Strobe
/SCAS	Column Address Strobe
/SWE	Write Enable
VDD	+2.5 Voltage power supply
VDDQ	+2.5 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	+2.5 Voltage Serial EEPROM Power Supply
EA0~EA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VDDID	VDD Identification Flag
VSS	Ground
/RESET	Reset enable
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	47	SDQS8	93	VSS	139	VSS
02	SDQ0	48	SA0	94	SDQ4	140	SDM8
03	VSS	49	SCB2	95	SDQ5	141	SA10
04	SDQ1	50	VSS	96	VDDQ	142	SCB6
05	SDQS0	51	SCB3	97	SDM0	143	VDDQ
06	SDQ2	52	SBA1	98	SDQ6	144	SCB7
07	VDD	53	SDQ32	99	SDQ7	145	VSS
08	SDQ3	54	VDDQ	100	VSS	146	SDQ36
09	NC	55	SDQ33	101	NC	147	SDQ37
10	/RESET	56	SDQS4	102	NC	148	VDD
11	VSS	57	SDQ34	103	NC	149	SDM4
12	SDQ8	58	VSS	104	VDDQ	150	SDQ38
13	SDQ9	59	SBA0	105	SDQ12	151	SDQ39
14	SDQS1	60	SDQ35	106	SDQ13	152	VSS
15	VDDQ	61	SDQ40	107	SDM1	153	SDQ44
16	*CK1	62	VDDQ	108	VDD	154	/SRAS
17	*/CK1	63	/SWE	109	SDQ14	155	SDQ45
18	VSS	64	SDQ41	110	SDQ15	156	VDDQ
19	SDQ10	65	/SCAS	111	SCKE1	157	/SCS0
20	SDQ11	66	VSS	112	VDDQ	158	/SCS1
21	SCKE0	67	SDQS5	113	NC	159	SDM5
22	VDDQ	68	SDQ42	114	SDQ20	160	VSS
23	SDQ16	69	SDQ43	115	SA12	161	SDQ46
24	SDQ17	70	VDD	116	VSS	162	SDQ47
25	SDQS2	71	*/SCS2	117	SDQ21	163	NC
26	VSS	72	SDQ48	118	SA11	164	VDDQ
27	SA9	73	SDQ49	119	SDM2	165	SDQ52
28	SDQ18	74	VSS	120	VDD	166	SDQ53
29	SA7	75	*/CK2	121	SDQ22	167	NC
30	VDDQ	76	*CK2	122	SA8	168	VDD
31	SDQ19	77	VDDQ	123	SDQ23	169	SDM6
32	SA5	78	SDQS6	124	VSS	170	SDQ54
33	SDQ24	79	SDQ50	125	SA6	171	SDQ55
34	VSS	80	SDQ51	126	SDQ28	172	VDDQ
35	SDQ25	81	VSS	127	SDQ29	173	NC
36	SDQS3	82	VDDID	128	VDDQ	174	SDQ60
37	SA4	83	SDQ56	129	SDM3	175	SDQ61
38	VDD	84	SDQ57	130	SA3	176	VSS
39	SDQ26	85	VDD	131	SDQ30	177	SDM7
40	SDQ27	86	SDQS7	132	VSS	178	SDQ62
41	SA2	87	SDQ58	133	SDQ31	179	SDQ63
42	VSS	88	SDQ59	134	SCB4	180	VDDQ
43	SA1	89	VSS	135	SCB5	181	EA0
44	SCB0	90	NC	136	VDDQ	182	EA1
45	SCB1	91	SDA	137	CK0	183	EA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

* Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on V_{DD} supply to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	36	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD	2.3	2.7	V	
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	V_{DDQ}/2-50mV	V_{DDQ}/2+50mV	V	1
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	VIH (DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	VIL (DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and /CK inputs	VIN (DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and /CK inputs	VID (DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and /CK inputs	VIX (DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) VOUT= VTT + 0.84V	I_{OH}	-16.8		mA	
Output Low Current (Normal strength driver) VOUT= VTT – 0.84V	I_{OL}	16.8		mA	
Output High Current (Half strength driver) VOUT= VTT + 0.45V	I_{OH}	-9		mA	
Output High Current (Half strength driver) VOUT= VTT - 0.45V	I_{OL}	9		mA	

Note:
1. Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled. TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of <=3nH.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Max.	Unit	Note
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK= tCK min DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	IDD0	3,180	mA	
Operating current - One bank Active-Read-Precharge; Burst=4; tRC=tRC min; CL=2.5; tCK=tCK min; VIN=VREF fro DQ,DQS and DM	IDD1	3,540	mA	
Percharge power-down standby current; All banks idle; Power –down mode; CKE = <VIL (max); tCK= tCK min VIN = VREF for DQ, DQS and DM	IDD2P	1,650	mA	
Precharge Floating standby current; CS# > =VIH (min); All banks idle; CKE > = VIH (min); tCK=133Mhz for DDR266 Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	IDD2F	2,010	mA	
Active power - down standby current; one bank active; power-down mode; CKE<= VIL (max); tCK = tCK min; VIN = VREF for DQ, DQS and DM	IDD3P	1,920	mA	
Active standby current; CS# >= VIH (min); CKE>=VIH (min); One bank active; active - precharge; tRC=tRASmax; tCK = tCK min; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	2,280	mA	
Operating current - burst read; Burst length = 2; reads; continuous burst; One bank active; address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min; 50% of data changing at every burst; Iout = 0 mA	IDD4R	4,710	mA	
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W	5,520	mA	
Auto refresh current; tRC = tRFC(min)	IDD5	5,070	mA	
Self refresh current; CKE <= 0.2V;	IDD6	558	mA	
Orerating current - Four bank operation; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7	8,040	mA	

Note: Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

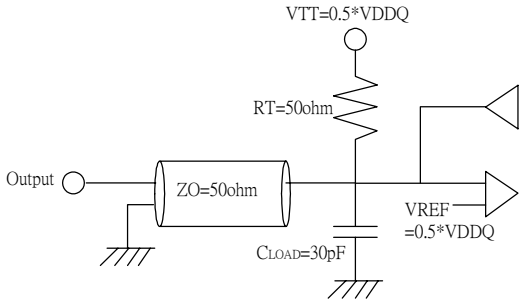
AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	2

Note: 1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation the AC and DC input specifications are relative to a VREF envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (VDD=2.5, VDDQ=2.5, TA=0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5*VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels (VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	VTT	V	
Output load condition	See Load Circuit		



Output Load circuit

Input/Output CAPACITANCE (VDD = 2.5V, VDDQ = 2.5V,TA = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (SA0~SA12, SBA0~SBA1, /SRAS, /SCAS, /SWE)	C_{IN1}	6	8	pF
Input capacitance (SCKE0, SCKE1)	C_{IN2}	5	7	pF
Input capacitance (/SCS0, /SCS1)	C_{IN3}	5	7	pF
Input capacitance (CK0, /CK0)	C_{IN4}	8	10	pF
Input capacitance (SDM0~SDM8)	C_{IN5}	12	14	pF
Data and DQS input/output capacitance (SDQ0~SDQ63)	C_{OUT1}	12	14	pF
Data input/output capacitance (SCB0~SCB7)	C_{OUT2}	12	14	pF

AC Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
Row cycle time	tRC	65		ns	
Refresh row cycle time	tRFC	75		ns	
Row active time	tRAS	45	120K	ns	
/RAS to /CAS delay	tRCD	20		ns	
Row active to Row active delay	tRP	20		ns	
Row active to Row active delay	tRRD	15		ns	
Write recovery time	tWR	15		ns	
Last data in to Read command	tWTR	1		tCK	
Col. Address to Col. Address delay	tCCD	1		tCK	
Clock cycle time	tCK	7.5	12	ns	
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK /CK	tDQSCK	-0.75	0.75	ns	
Output data access time from CK /CK	tAC	-0.75	0.75	ns	
Data strobe edge to output data edge	tDQSQ		0.5	ns	
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	tCK	
DQS-in setup time	tWPRES	0		ns	2
DQS-in hold time	tWPRE	0.25		tCK	
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
DQS-in cycle time	tDSC	0.9	1.1	tCK	
Address and Control input setup time	tIS	0.9		ns	
Address and Control input hold time	tIH	0.9		ns	
Data-out high-impedance time from CK, /CK	tHZ	-0.75	0.75	ns	
Data-out low-impedance time from CK, /CK	tLZ	-0.75	0.75	ns	
Mode register set cycle time	tMRD	15		ns	
DQ & DM setup time to DQS	tDS	0.5		ns	
DQ & DM hold time to DQS	tDH	0.5		ns	
DQ & DM input pulse width	tDIPW	1.75		ns	
Power down exit time	tPDEX	7.5		ns	
Exit self refresh to non-read command	tXSNR	75		ns	
Exit self refresh to read command	tXSRD	200		tCK	
Refresh interval time	tREFI	7.8		us	1
Clock half period	tHP	tCLmin or tCHmin		ns	
Data hold skew factor	tQHS		0.75	ns	
DQS write postamble time	tWPST	0.4	0.6	tCK	3

Note: 1. Maximum burst refresh of 8

2. The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The Maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are ≧45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	SA_{10}/AP	SA_0~SA_9, SA_{11}, SA_{12}	Note
Register	Extended Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (SA_0~SA_9, SA_{11})	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (SA_0~SA_9, SA_{11})	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
					L	V	V	V				
	Exit		L	H	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
					L	H	H	H				
	Exit		L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No Operation Command			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note:
1. OP Code: Operand Code. A0 ~ A12 & BA0 ~ BA1: Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM. The automatical precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1: Bank select addresses. If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected. If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected. If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected. If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command cannot be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in is masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	DDR SDRAM	07
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	11	0B
5	# of Module Rows on this Assembly	2 bank	02
6	Data Width of this Assembly	72bits	48
7	Data Width of this Assembly	0	00
8	VDDQ and Interface Standard of this Assembly	SSTL 2.5V	04
9	DDR SDRAM Cycle Time at CAS Latency=2.5	7.5ns	75
10	DDR SDRAM Access Time from Clock at CL=2.5	0.75ns	75
11	DIMM configuration type (non-parity, Parity, ECC)	ECC	02
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary DDR SDRAM Width	X4	04
14	Error Checking DDR SDRAM Width	X4	04
15	Min Clock Delay for Back to Back Random Column Address	tCCD=1CLK	01
16	Burst Lengths Supported	2,4,8	0E
17	# of banks on each DDR SDRAM device	4 bank	04
18	CAS Latency supported	2, 2.5	0C
19	CS Latency	0 CLK	01
20	WE Latency	1 CLK	02
21	DDR SDRAM Module Attributes	Registered address & control inputs and on-card DLL	26
22	DDR SDRAM Device Attributes: General	+/-0.2V voltage tolerance	00
23	DDR SDRAM Cycle Time CL=2.0	10ns	A0
24	DDR SDRAM Access from Clock CL=2.0	0.75ns	75
25	DDR SDRAM Cycle Time CL=1.5	-	00
26	DDR SDRAM Access from Clock CL=1.5	-	00
27	Minimum Row Precharge Time (tRP)	20ns	50
28	Minimum Row Active to Row Activate delay (tRRD)	15ns	3C
29	Minimum RAS to CAS Delay (tRCD)	20ns	50
30	Minimum active to Precharge time (tRAS)	45ns	2D
31	Module ROW density	512MB	80
32	Command/Address Input Setup Time	0.9ns	90
33	Command/Address Input Hold Time	0.9ns	90
34	Data Signal Input Setup Time	0.5ns	50
35	Data Signal Input Hold Time	0.5ns	50
36-61	Superset Information	-	00
62	SPD Data Revision Code	-	00
63	Checksum for Bytes 0-62	-	11
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F

72	Manufacturing Location	T	54						
73-90	Manufacturers Part Number	TS128MDR72V6L5	54	53	31	32	38	4D
			44	52	37	32	56	36
			4C	35	20	20	20	20
91-92	Revision Code	-	-						
93-94	Manufacturing Date	By Manufacturer	Variable						
95-98	Assembly Serial Number	By Manufacturer	Variable						
99-127	Manufacturer Specific Data	-	-						
128~255	Unused Storage Locations	Undefined	-						